ICSCRM 2011 の報告（デバイス関連）

京都大学 工学研究科 電子工学専攻

木本 恒暢

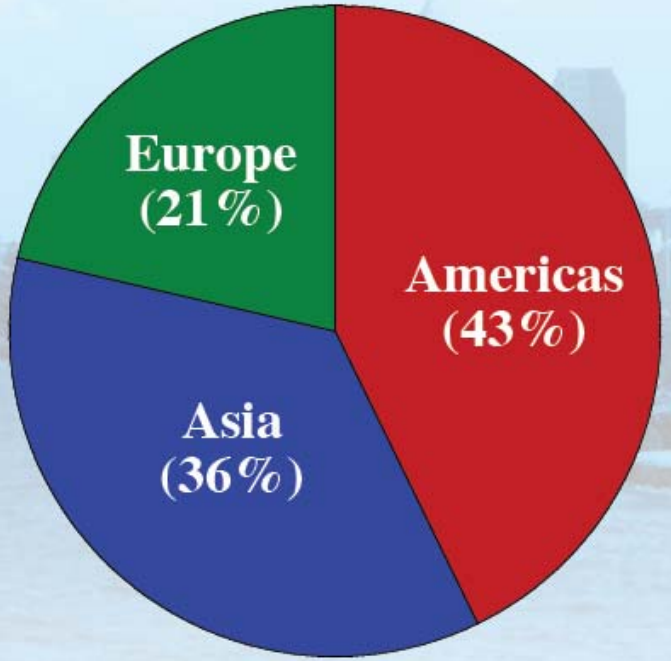
2011. 11. 7

ICSCRM 2011 参加者の分布

ICSCRM 2011 Registrations

(As of Tuesday Sept. 12)

603 Total conference attendees representing 27 countries (including 87 students).



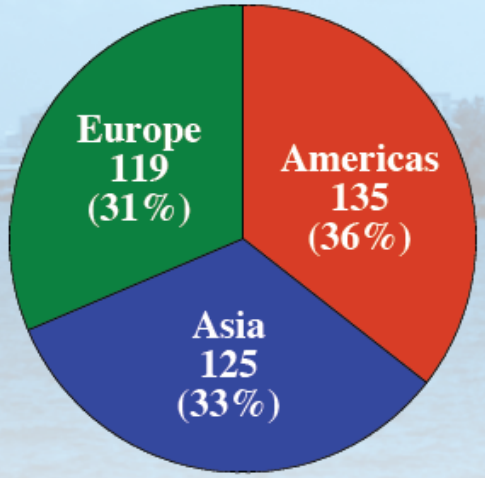
ICSCRM 2011
Cleveland, Ohio • USA

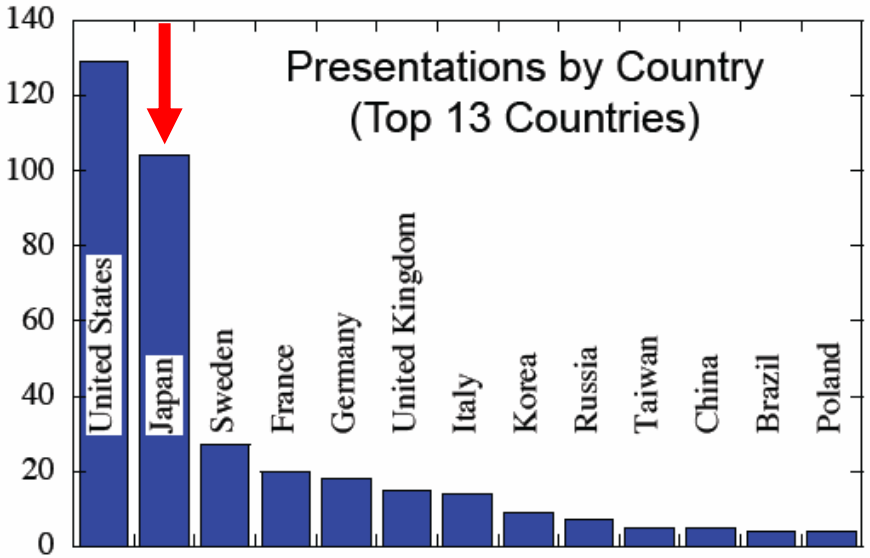
ICSCRM 2011 論文数の分布

Technical Program

379 Presentations were selected from 426 total submitted abstracts
- 127 Oral Presentations, 252 Poster Presentations
- 25 Invited Speakers, 5 Invited Posters
- 2 Late News Speakers, 29 Late News Posters

Presentations by Region





ICSCRM 2011
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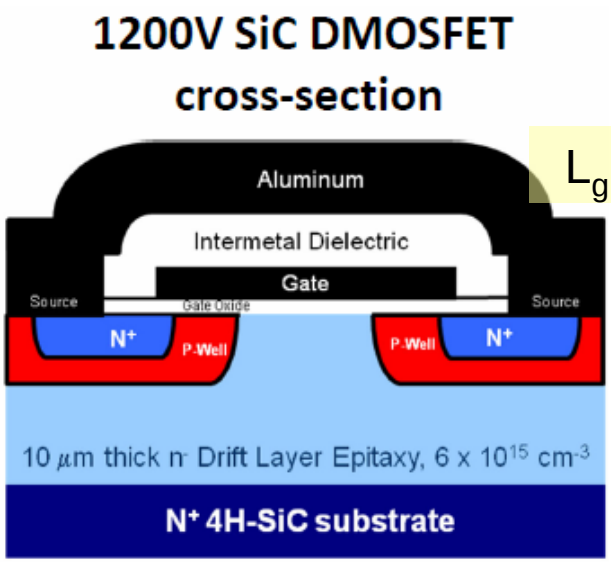
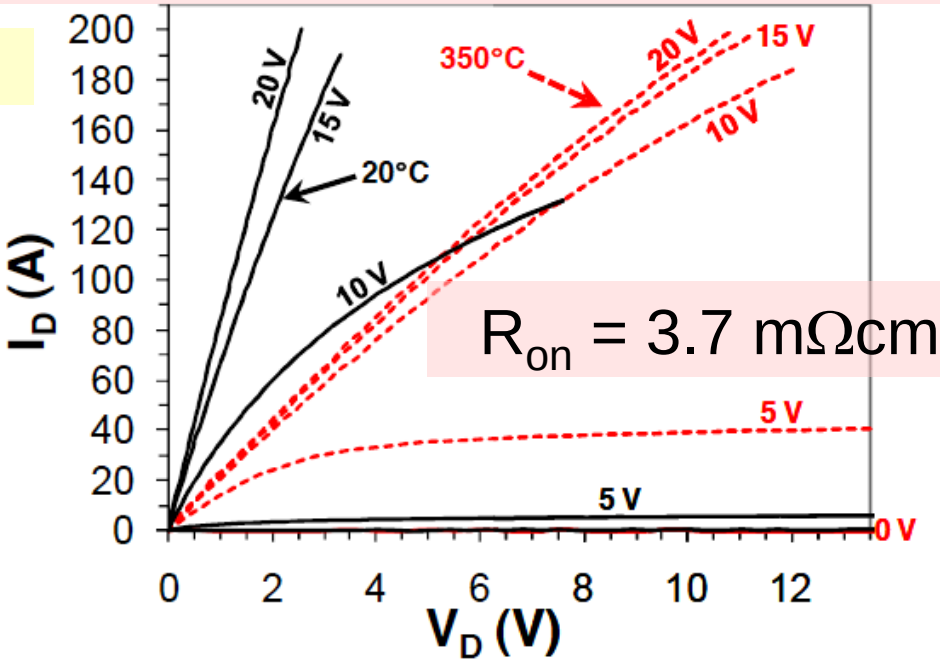
1200 V – 200 A DMOSFET (Cree)



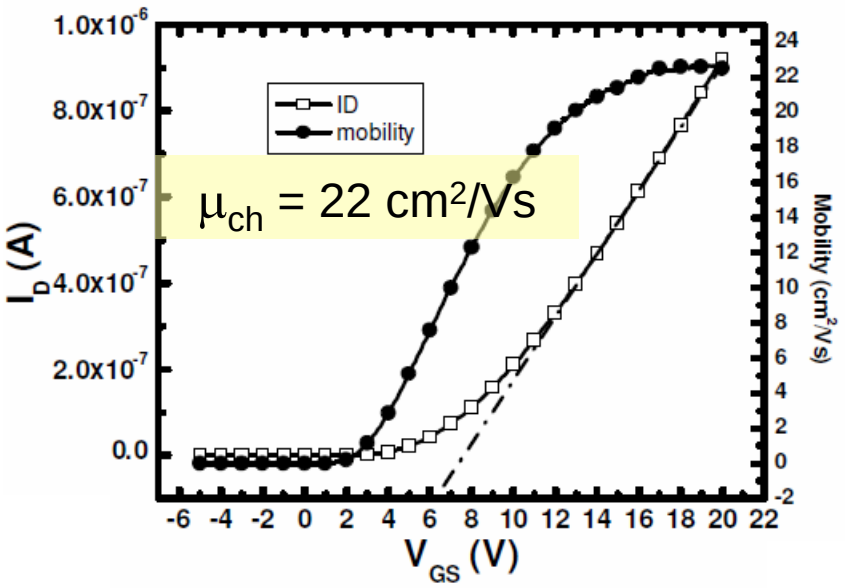
L_g = 0.5 μm

V_{DS} = 2.58 V @ 200 A (V_{GS} = 20 V)

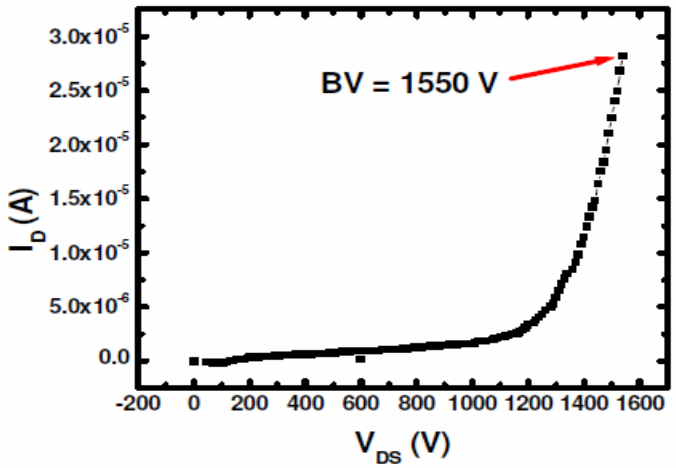


R_{on} = 3.7 mΩcm²

7 mm x 8 mm (active area: 0.4 cm²)



μ_{ch} = 22 cm²/Vs



690 V – 1.0 mΩcm^2 トレンチMOSFET (ローム)

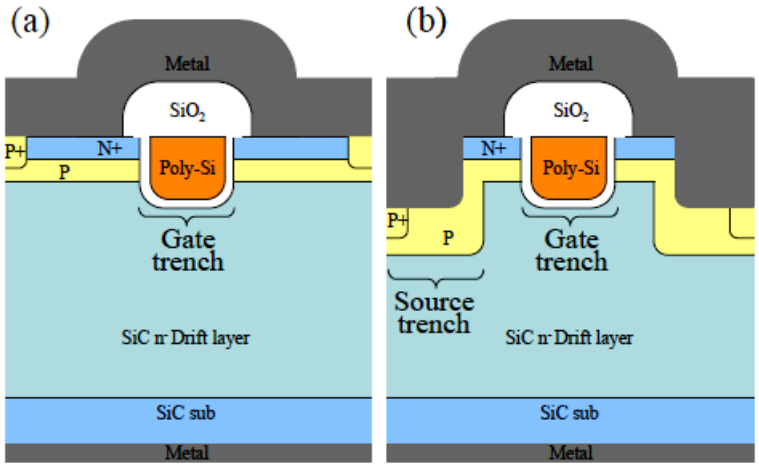


Figure 1 Schematics cross section of (a) conventional single-trench structure and (b) double-trench structure with source trench and gate trench.

1.6 mm x 1.6 mm (active area: 0.014 cm^2)

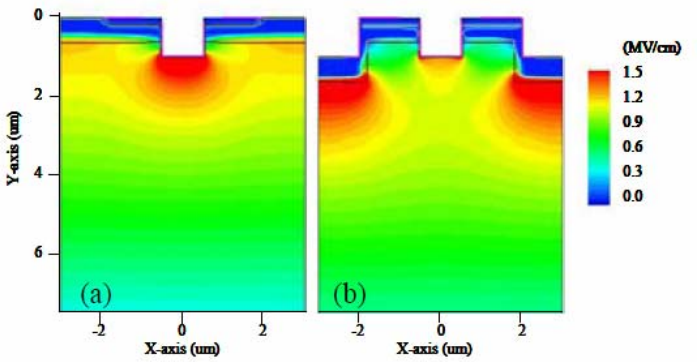


Figure 2 The electric field distribution of device cross section on the epi layer at V_{ds} = 600V and V_{gs} = 0V. (a) single-trench structure. (b) double- trench structure.

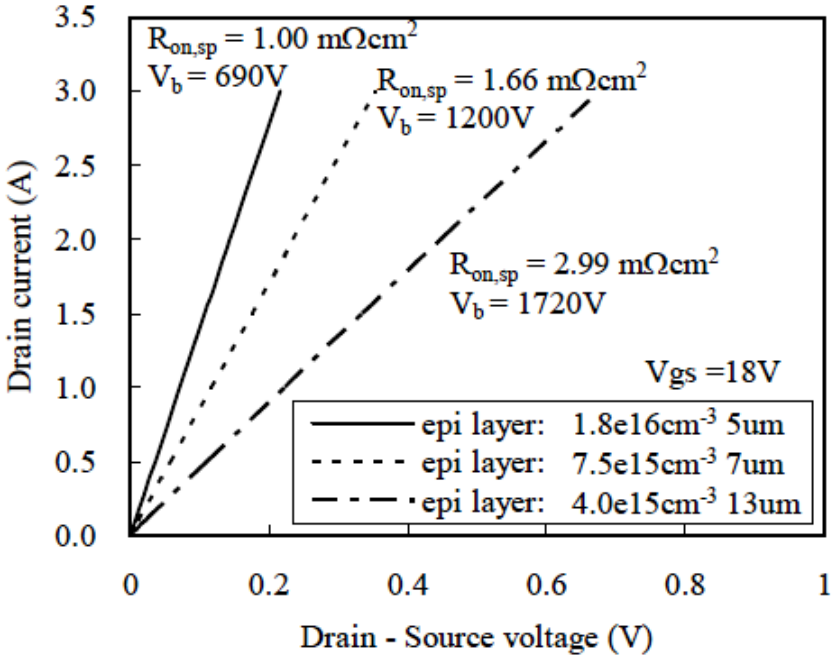


Figure 4 $I_d - V_{ds}$ characteristics of double-trench MOSFETs in case of V_{gs} = 18 V. The chip size is 1.6 mm x 1.6 mm. Active area is 0.01422 cm^2.

690 V – 1.0 mΩcm² トレンチMOSFET (ローム)

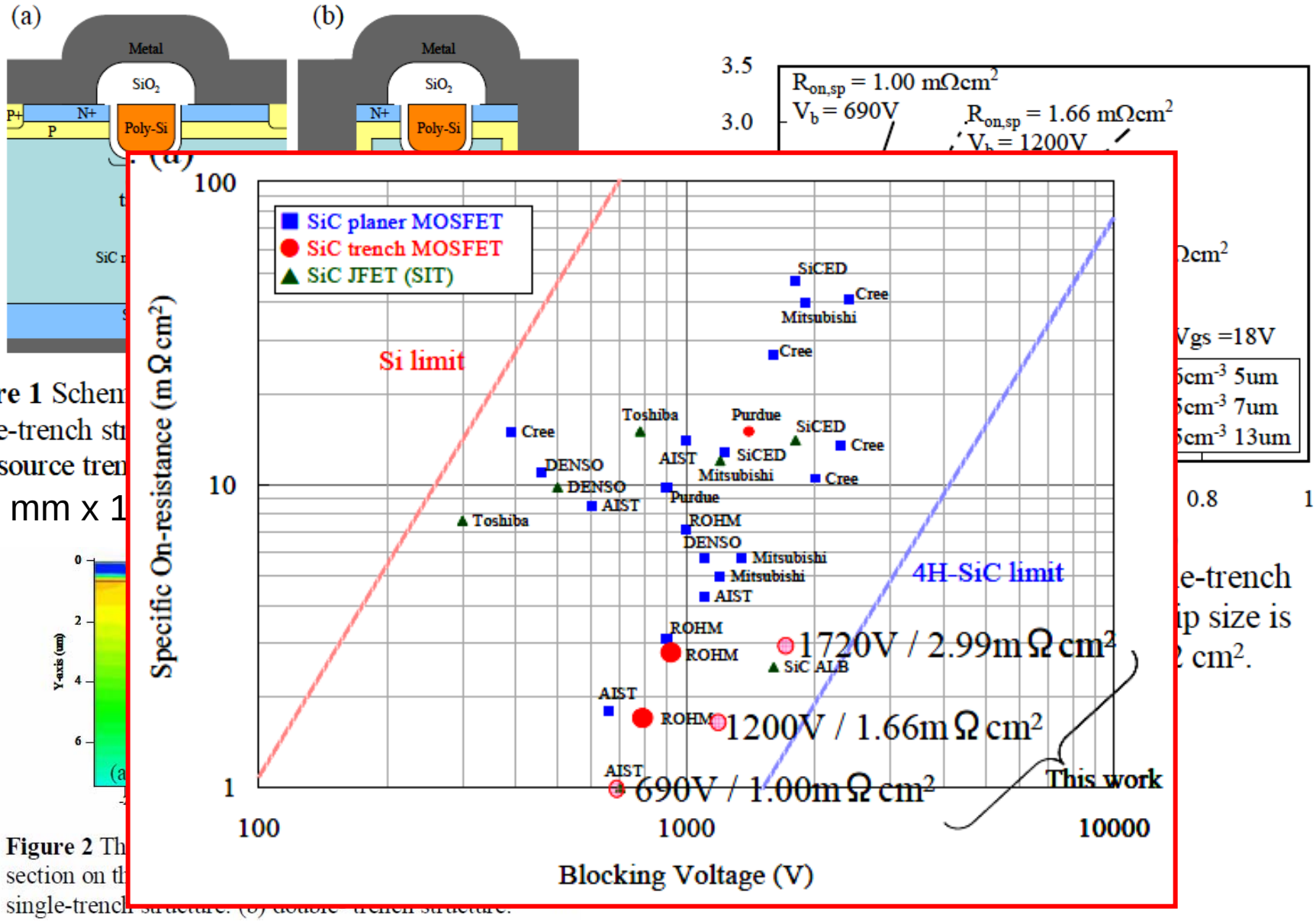


Figure 1 Schem
single-trench str
with source tren
1.6 mm x 1

Figure 2 Th
section on th
single-trench structure. (b) double-trench structure.

高温 (> 250°C) パワーモジュール (APEI)

1200 V, > 100 A, > 250°C のパワーモジュールを開発

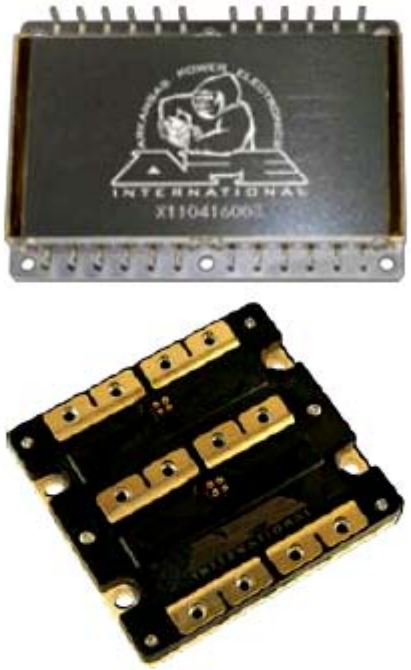


Fig. 1. APEI, Inc.'s high power (1200V and >100A) SiC power module products with (top) hermetically sealed, high reliability option (APE HT-1000 series) and (bottom) commercial, ultra-lightweight low profile option (APE HT-2000 series).

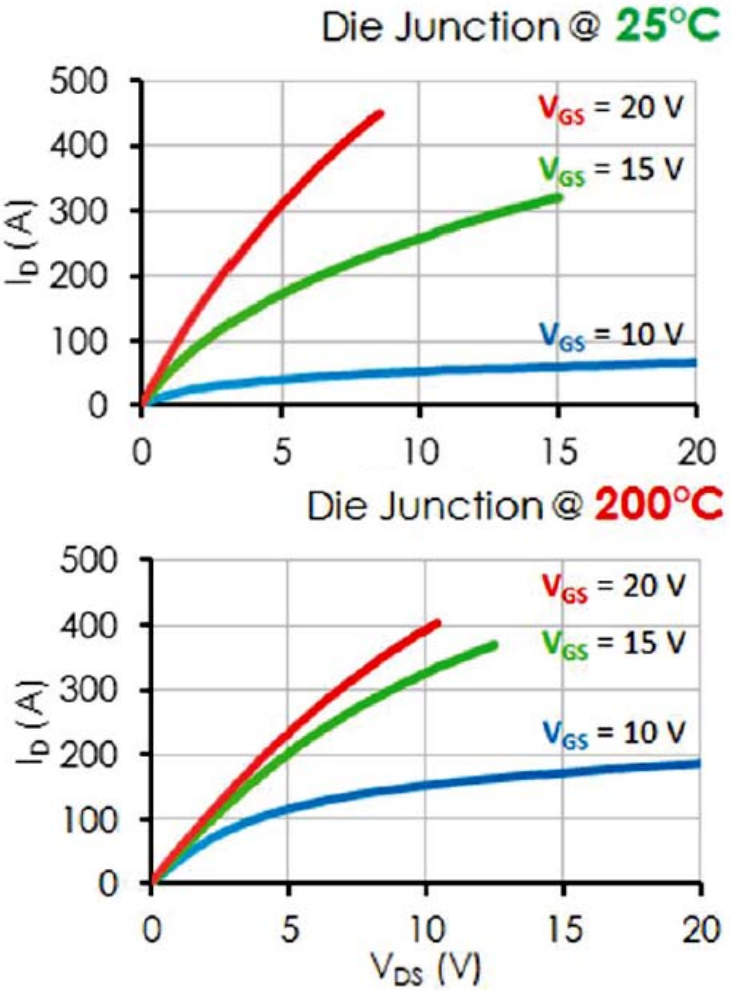


Fig. 3. APE HT-2000 power module output curves from 25 °C to 200 °C in a half-bridge configuration (single switch position shown) with 1200V SiC power MOSFETs [1].

SiC Solid-State Disconnect (United SiC)

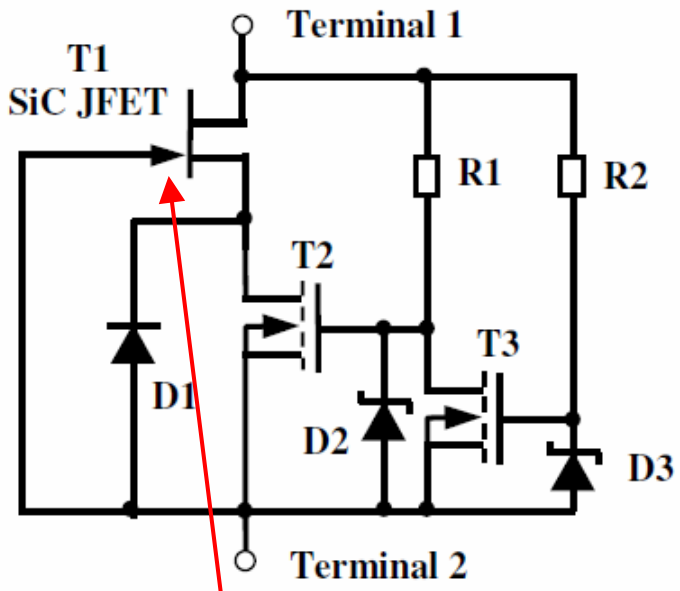
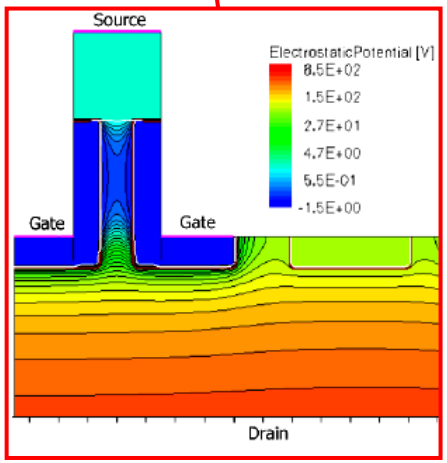
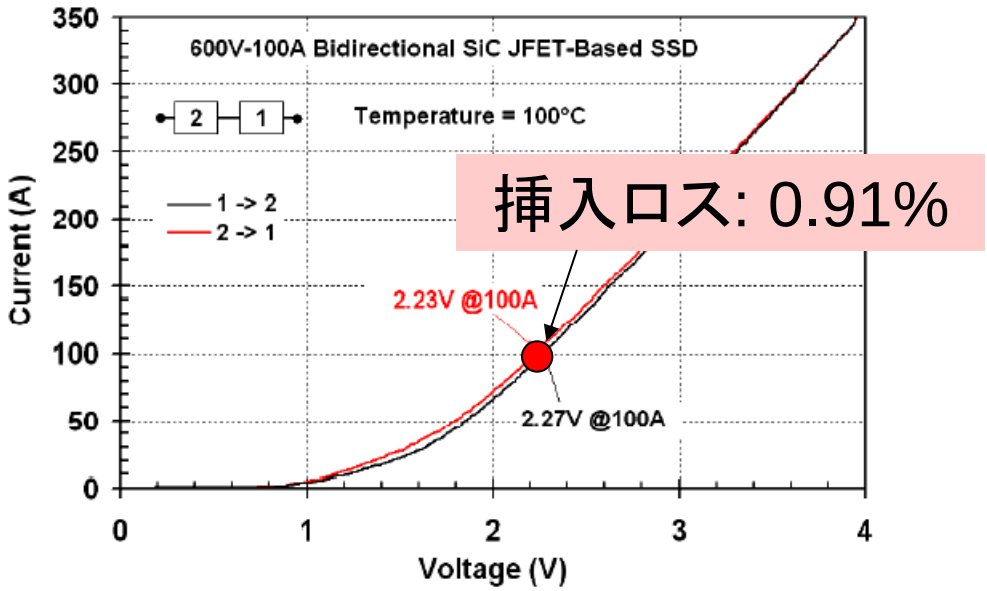


Fig.1. Circuit schematic diagram of the unidirectional SiC JFET based solid-state disconnect.



定常出力 25 kW
ピーク出力 180 kW

Fig.2. Photograph of a unidirectional 100A-600V SiC SSD prototype for 150kW bi-directional inverter system applications.



挿入ロス: 0.91%

Fig.3. DC characteristics of the bi-directional SSD for current flow in both directions at 100°C heat-sink temperature.

30 kW/L 高密度変換器 (FUPET他)

Table 1 Inverter specications

Output power	15 kW
Input	DC 600 V
Output	3ϕ – AC 400 V (60 Hz)
Switching frequency	8 kHz
Dead time	0.75 μs
Power factor	0.85
Inverter size	500 cc (15 cm x 9 cm x 3.7 cm)
FETs	SJEC120R025 (1200 V, Rds=25 mΩ)
Diodes	SDC30S120 (1200 V, 30 A)

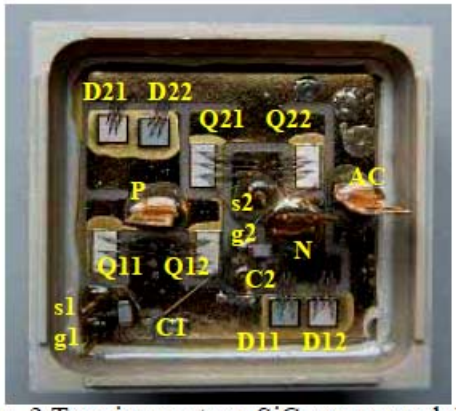


Fig. 2 Two-in-one-type SiC power module.

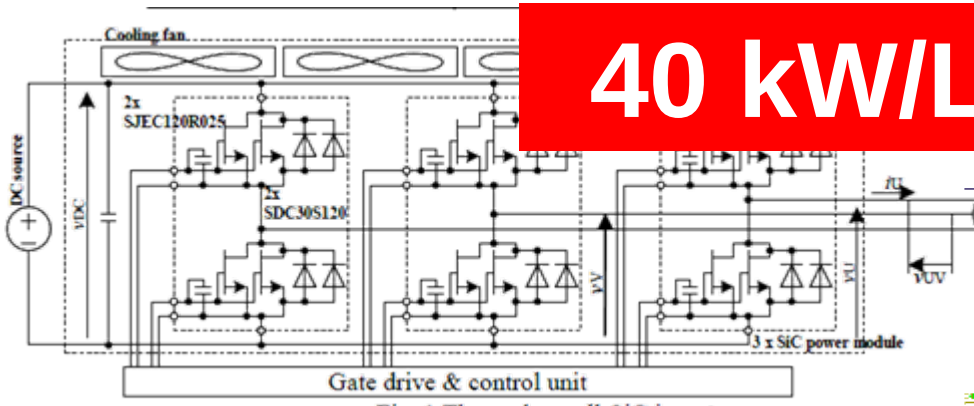


Fig. 1 Three-phase all-SiC inverter.

40 kW/L

1200 V – 25 A SiC JFETs
1200 V – 30 A SiC SBDs

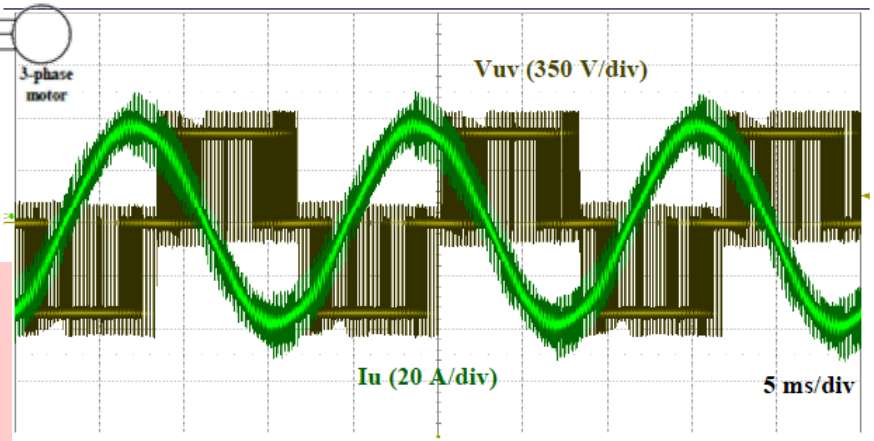


Fig. 4 Waveforms of inverter voltage and motor current.

15 kW (f = 8 kHz) 3相インバータ
効率: > 99%
出力電力密度: 30 kW/L (30 W/cc)

1 MW級変換器 (Cree/Powerex)

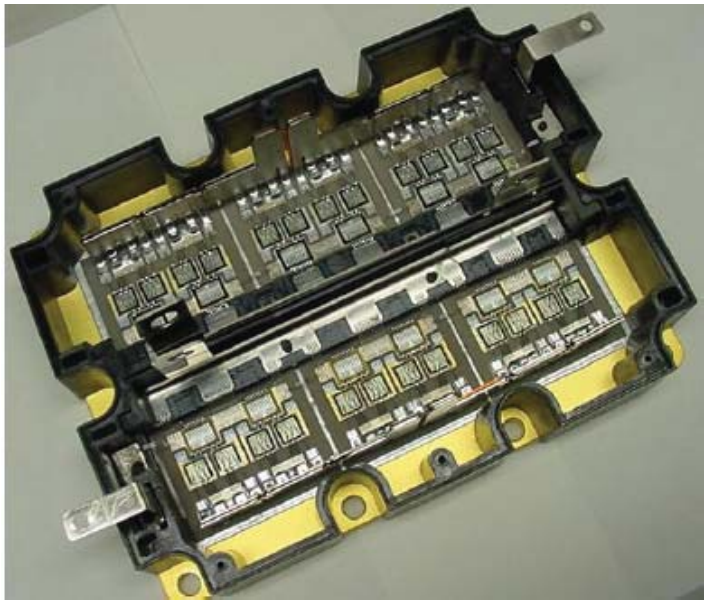


Fig. 3. Internal layout of the 10 kV, 120 A half H-bridge module containing 12 MOSFETs and 6 JBS diodes for each switch.

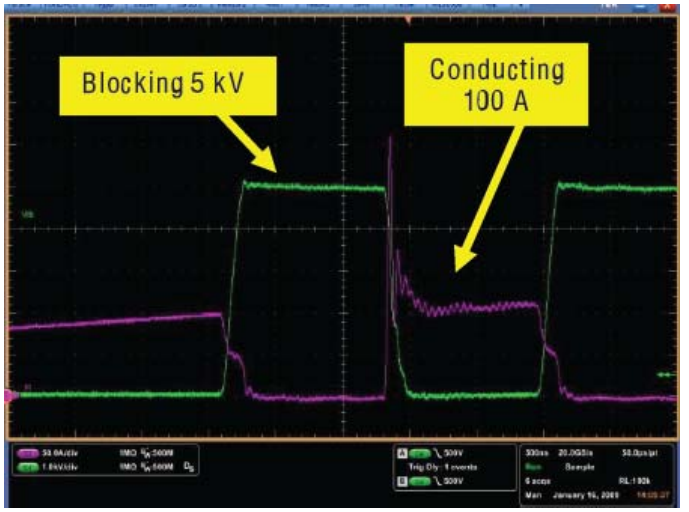


Fig. 5. Double pulse switching 5 kV and 100 A using the upper switch in the 10 kV, 120 A SiC half H-bridge MOSFET module shows fast 200 nsec transtions.

10 kV – 10 A SiC MOSFET x 12
10 kV – 20 A SiC JBS x 6

1 MW Solid-State Power Substation
効率: 97%
サイズ: 1/2, 重量: 1/4 (Si比)

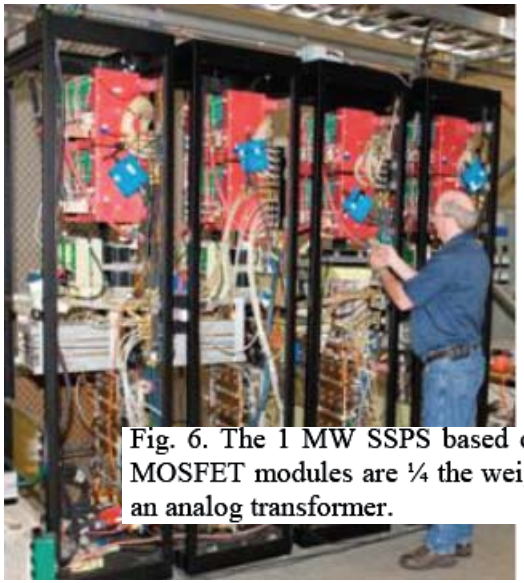


Fig. 6. The 1 MW SSPS based on 10 kV SiC power MOSFET modules are ¼ the weight and ½ the size of an analog transformer.

600 V級SBDのオン電圧低減の試み

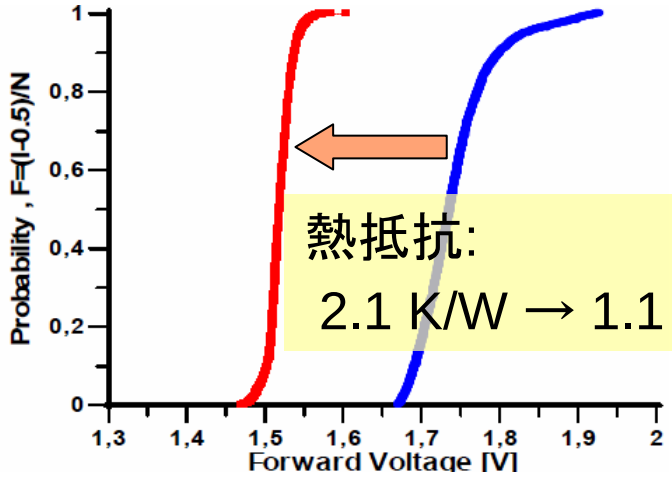
研磨による薄ウェハ化 (Infineon)

Fig. 1: Schematic drawing of the grinding principle used

ウェハ厚さ

350 μm → 110 μm

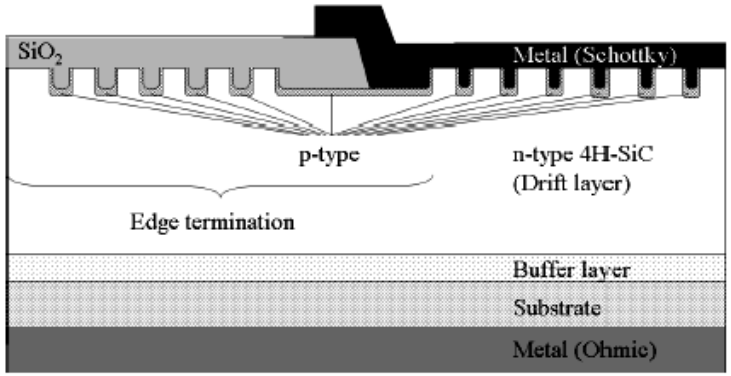
オン電圧 (620 A/cm^2) : 1.7 V → 1.5 V

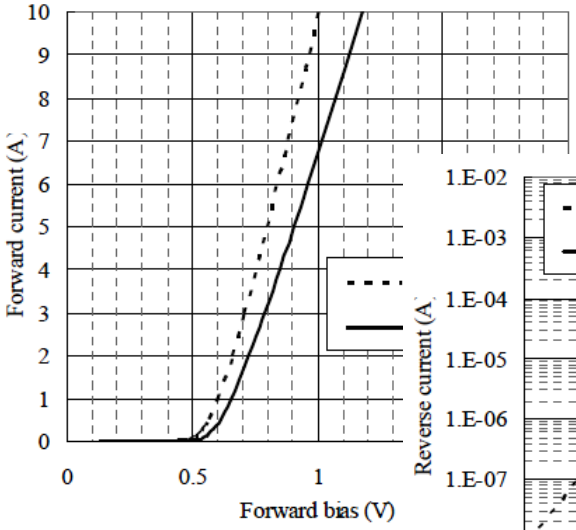


熱抵抗:

2.1 K/W → 1.1 K/W

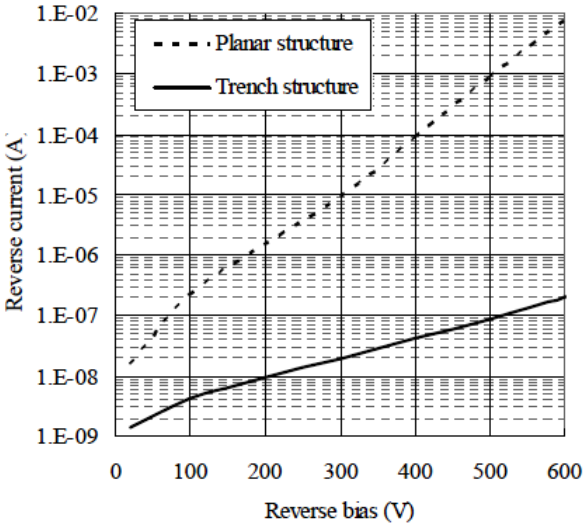
トレンチ構造の活用 (ローム)





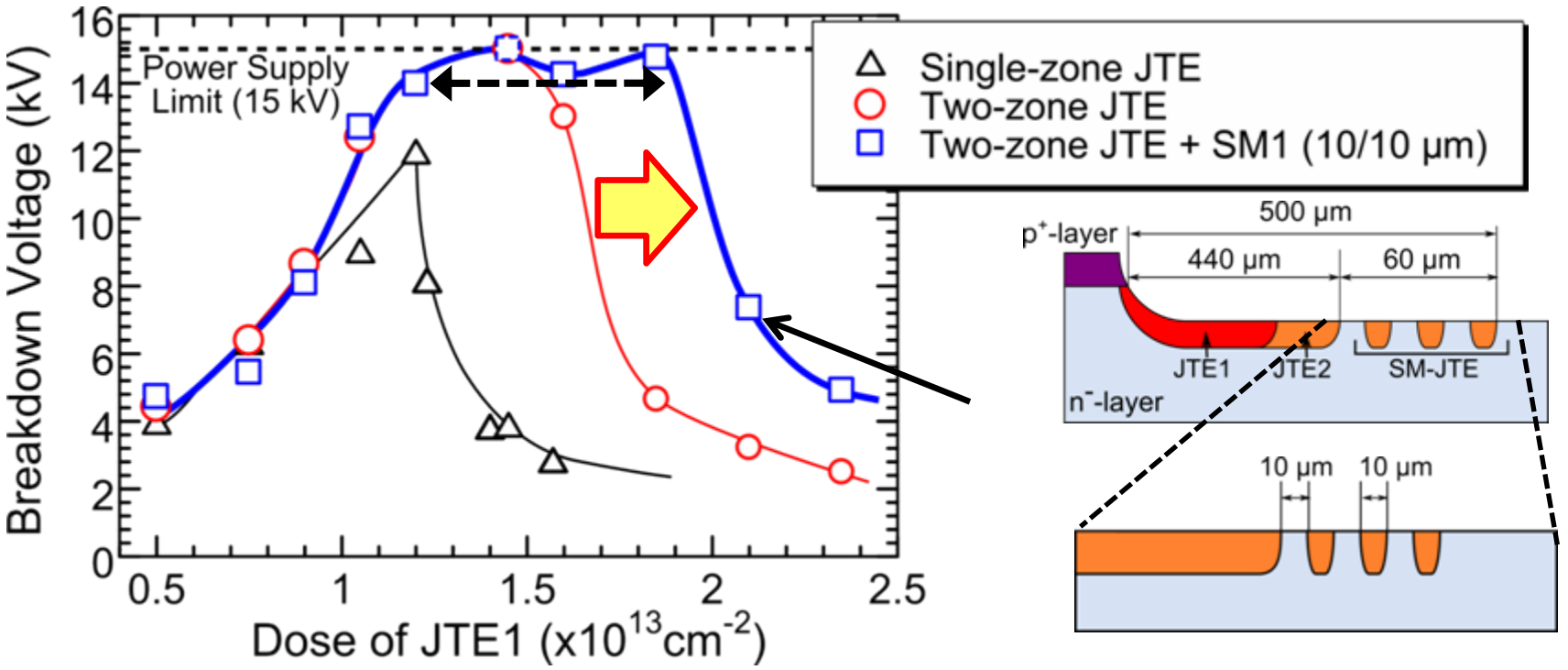
Moショットキー

(ϕ_B = 0.85 eV)



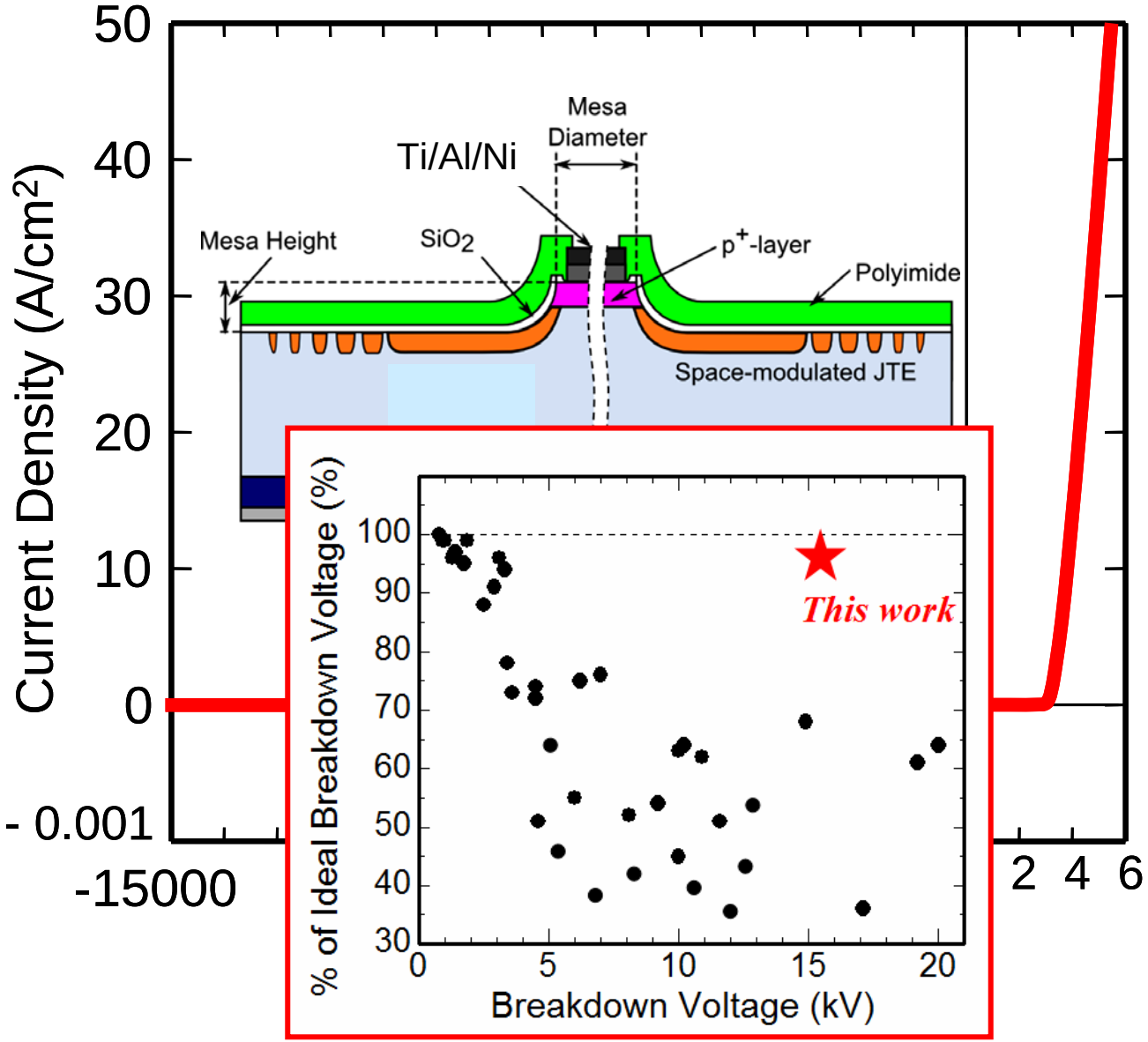
高耐圧デバイス用JTE構造の改良 (京都大)

耐圧のJTEドーズ量依存性（メサ形PiNダイオード）



Two-zone JTE + SM1 (空間変調JTE):
最適ドーズの幅が広い

JTE構造改良による理想的な耐圧の達成 (京都大)



理想耐圧(一次元):

16.1 kV

(147 μm, 7x10^{14} cm^{-3})

実測耐圧:

15.4 kV

(95%)

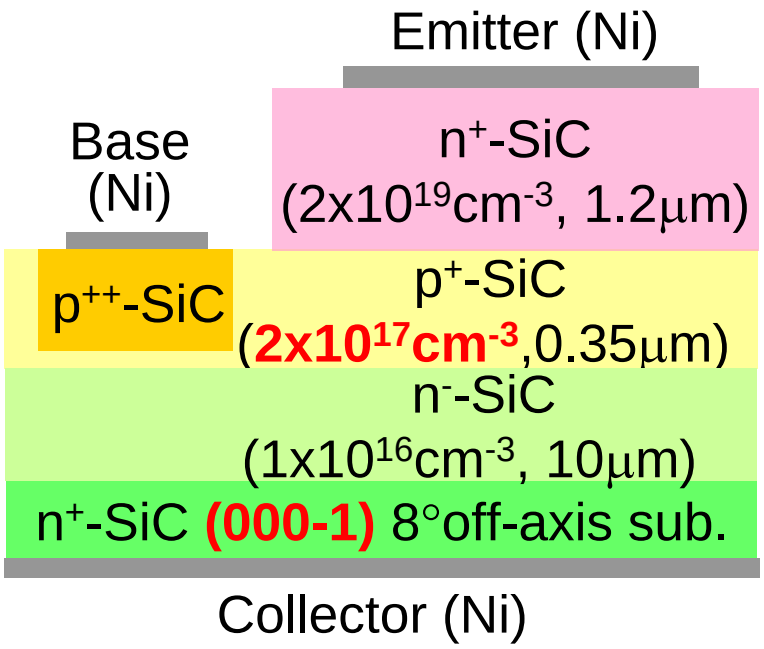
p^{+}型アノード:

Al^{+}イオン注入で形成

電界集中緩和:

メサ + Al^{+}注入JTE(空間変調)

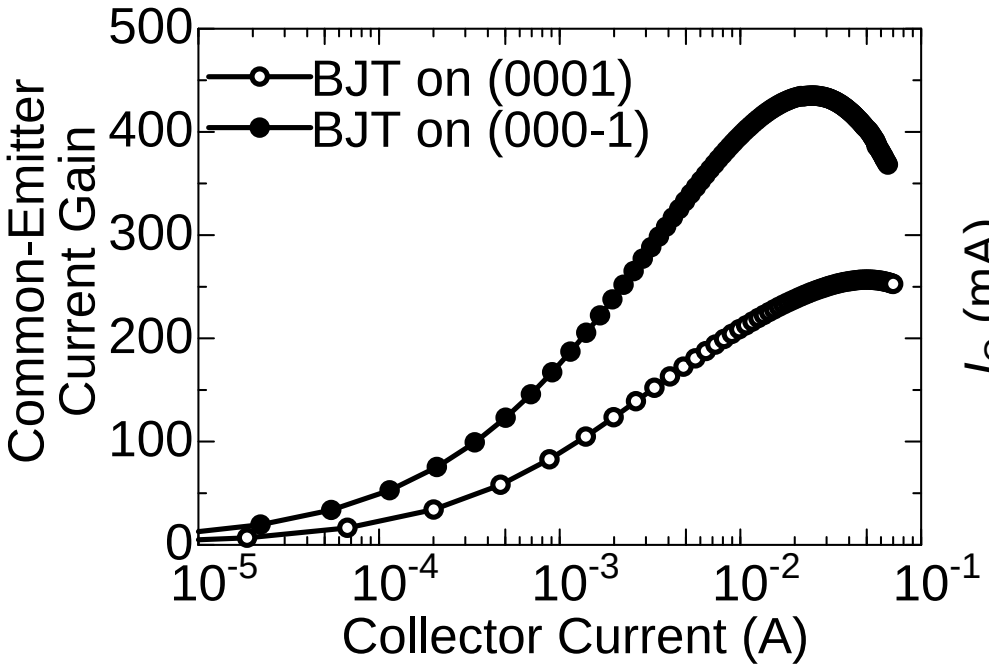
高電流利得BJTの作製プロセス (京都大)

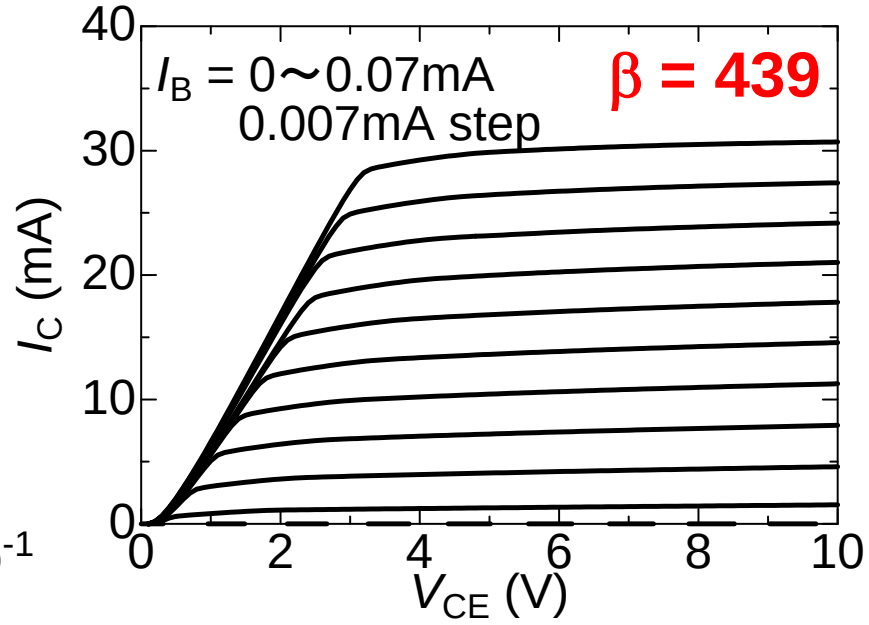


*Note
Doping concentration of p-SiC base is lower by a factor of 5.

- Emitter & Base Epitaxy
- Double-Mesa Formation (RIE)
- Base Ion Implantation
- Oxidation (1150ºC 15min)
- Activation Anneal @ 1800ºC
- Oxidation (1150ºC 15min)
- Surface Passivation
- Metal Deposition (Ni)
- Metallization Anneal @ 950ºC

高電流利得BJTの実現 (京都大)

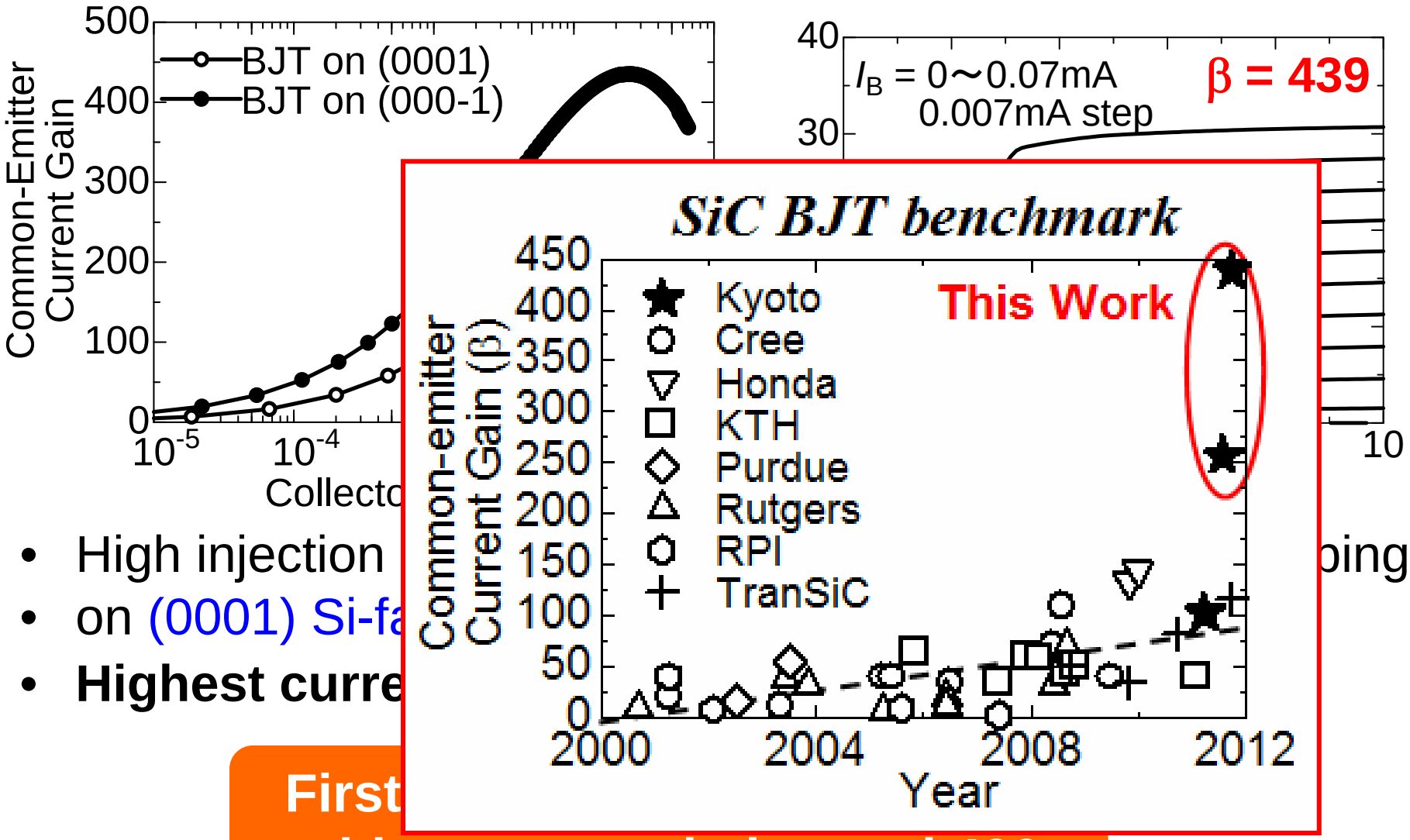




- High injection mode at low I_C due to the lower base doping
- on (0001) Si-face β = 257 → on (000$\bar{1}$) C-face β = 439
- **Highest current gain ever reported**

First operation of C-face BJTs with current gain beyond 400

高電流利得BJTの実現 (京都大)



- High injection
- on (0001) Si-fa
- **Highest curre**

First
with current gain beyond 400

6.5 kV – 2.5 mΩcm² サイリスタ (GeneSiC)

ベベルメサによる接合終端

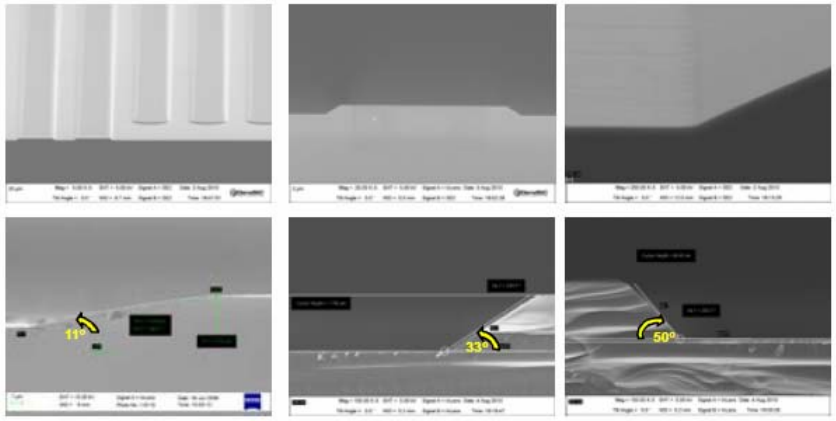
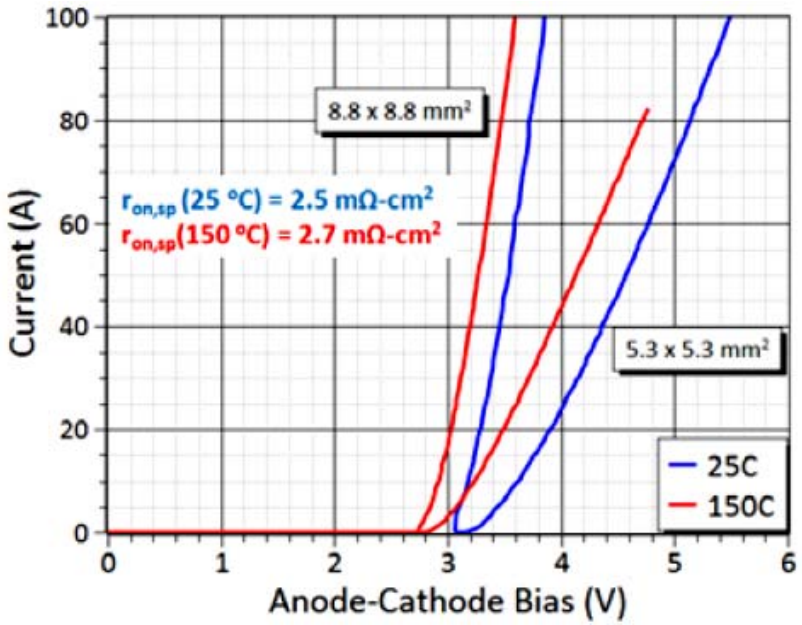
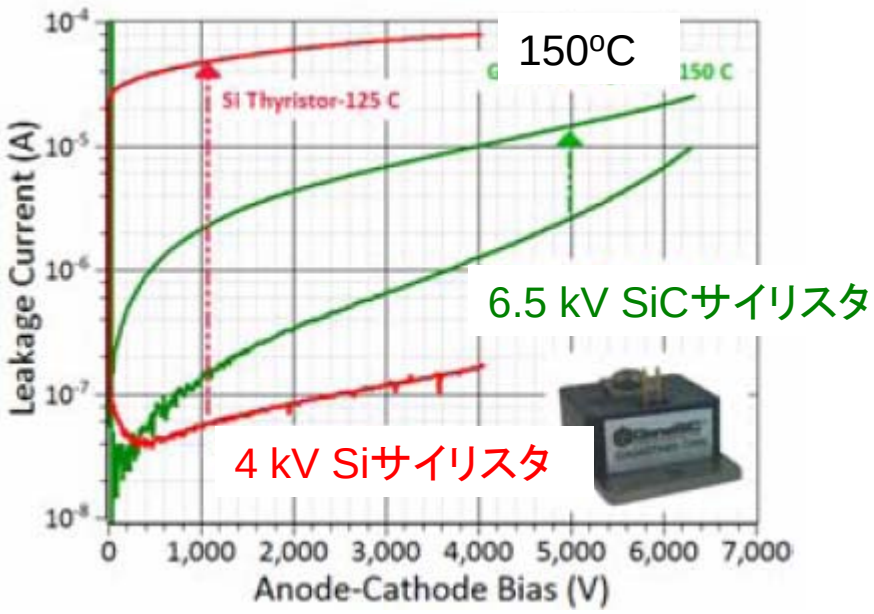
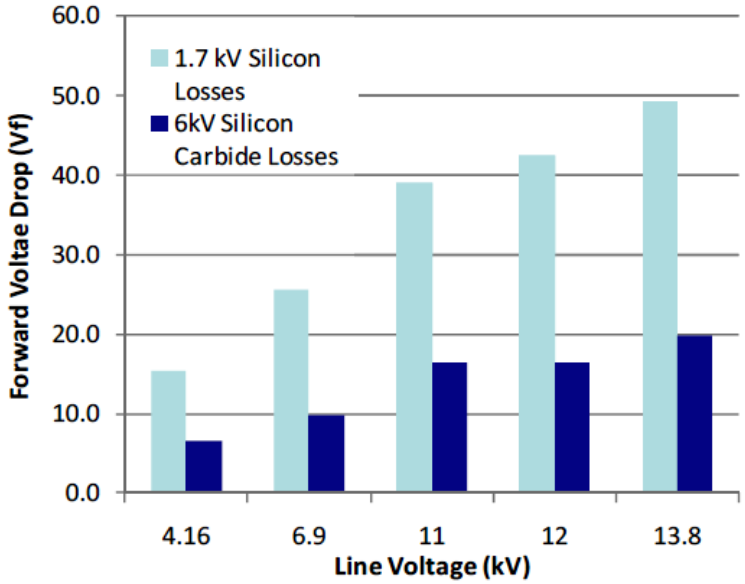


Figure 1: Cross-sectional SEMs of SiC Mesas etched with arbitrarily chosen sidewall slopes.

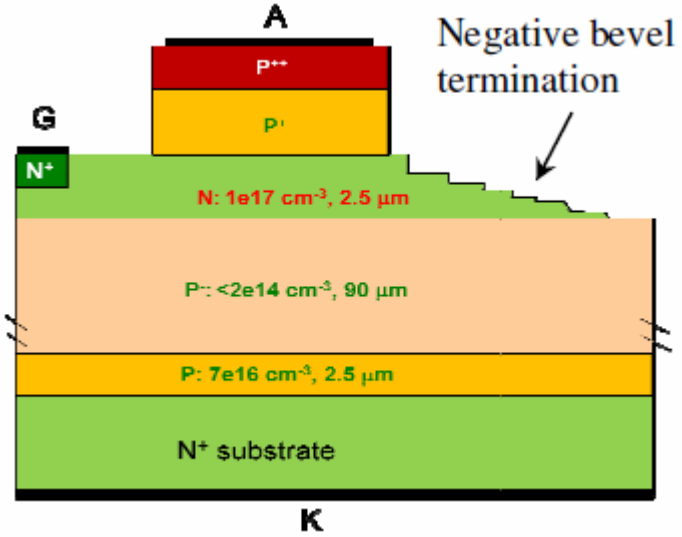


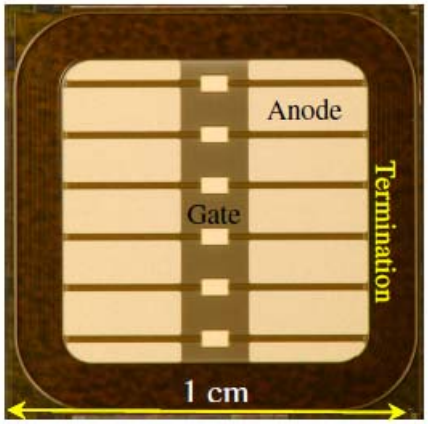




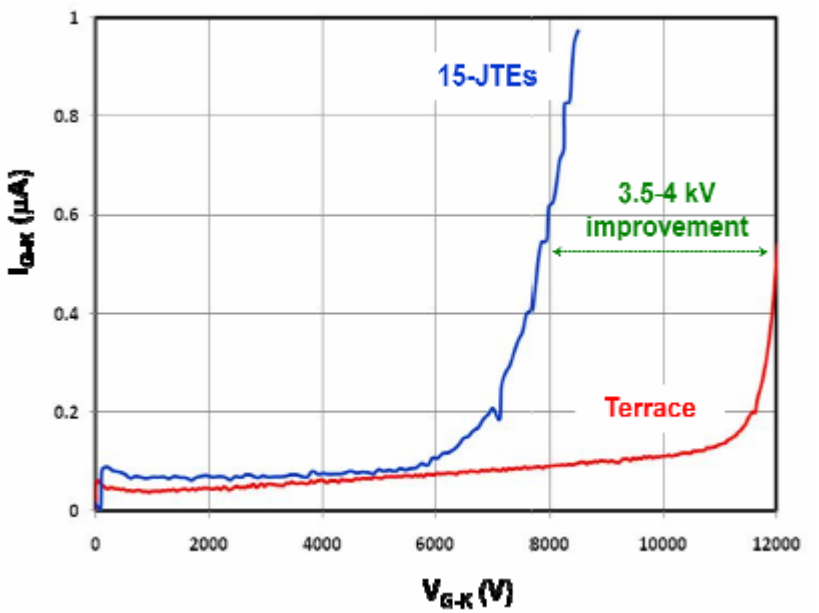
12 kV – 100 A サイリスタ (Cree)

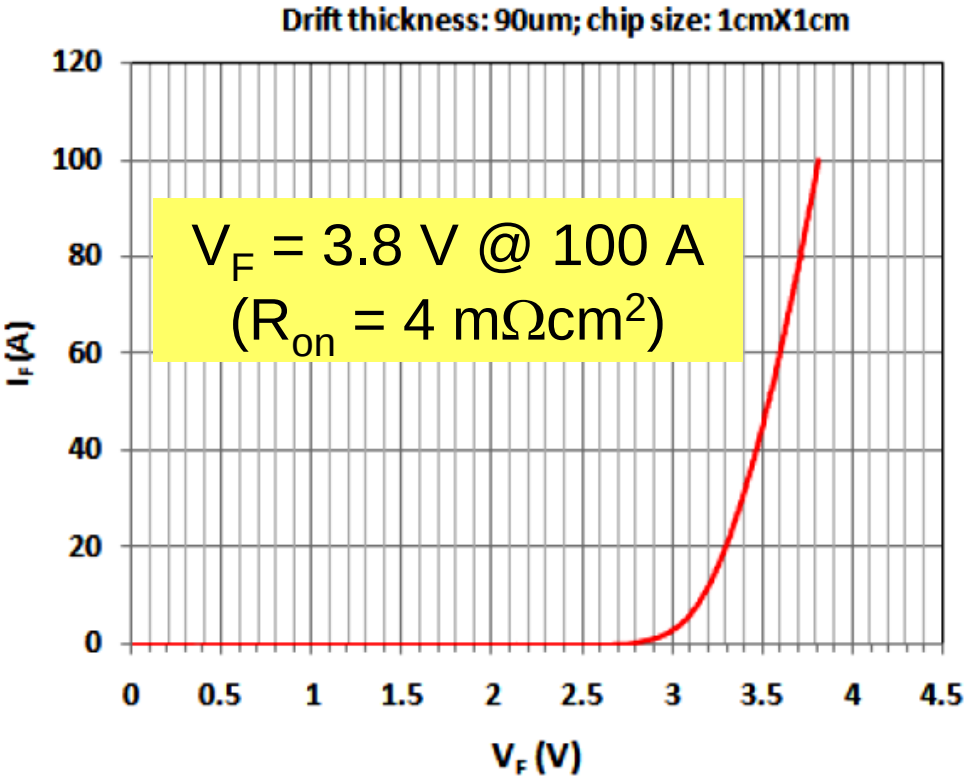
ネガティブベベルによる接合終端





1 cm x 1 cm
(termination: 600 µm)



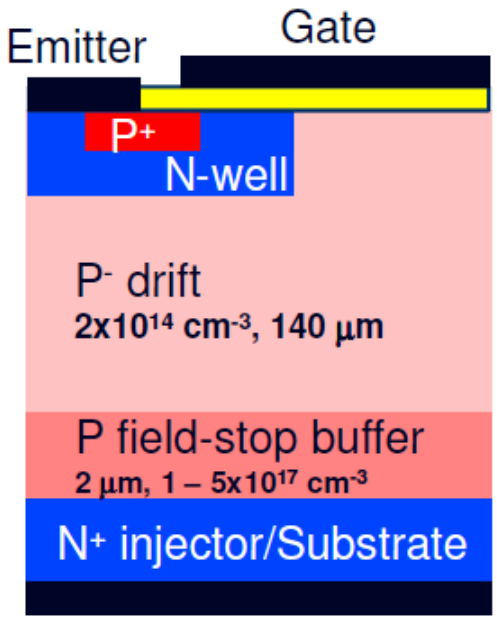


超高耐圧IGBT (Cree)

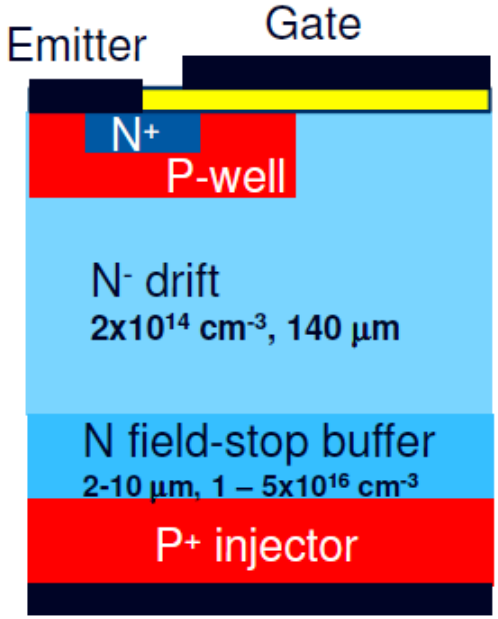
- **Possibility of Ultra-High Voltage devices**
  - **Reduction in # of series devices in high voltage stacks**
  - **Increased reliability**
  - **Silicon thyristors limited to ~ 11 kV**

4H-SiC IGBT structures
(Based on SiC DMOSFETs)

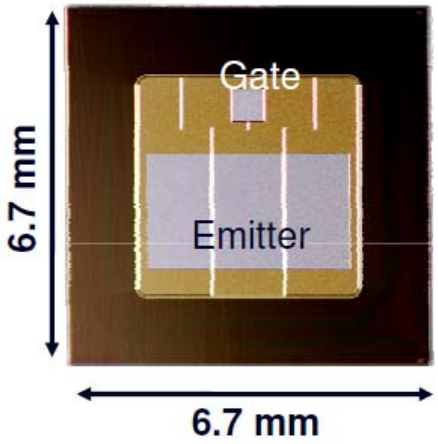
arpa·e



SiC P-IGBT structure



SiC N-IGBT structure

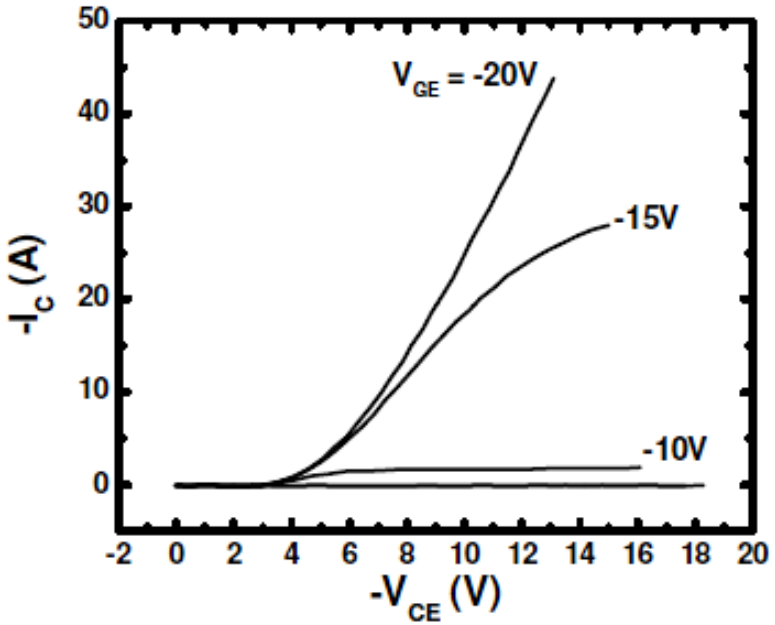


Chip size: 6.7 mm x 6.7 mm
Active area: 0.16 cm²
Target current: 5 A (30 A/cm²)

15 kV pチャネルIGBT (Cree)

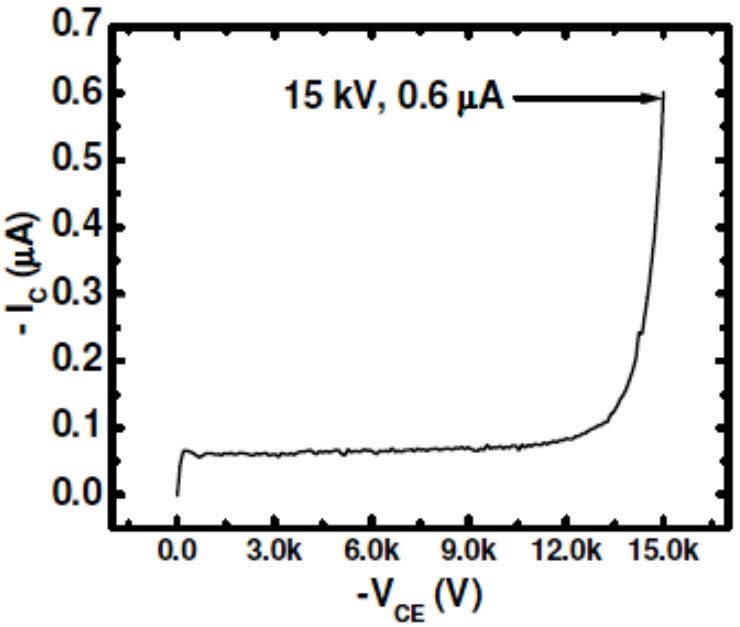
4H-SiC *P-IGBT* Characteristics (RT)

Highest BV reported in semiconductor switches!



V_F = 5.8V @ 5 A, V_{GE} = -20V
= 11.2 V @ 32 A (200 A/cm²)

$R_{on,sp}$ = 24 mΩ-cm²
(V_{GE}=-20V, V_{CE}=-11.2V)

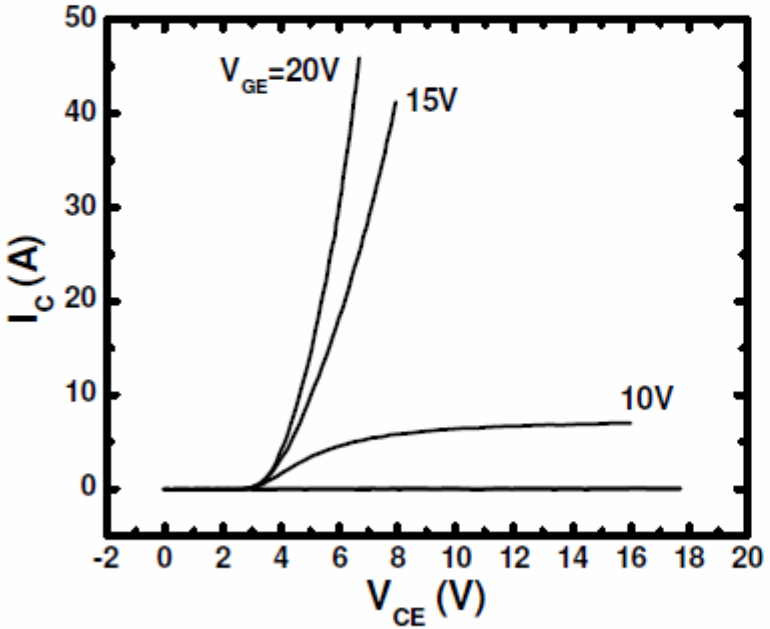


15 kV blocking (V_{GE}=0V)

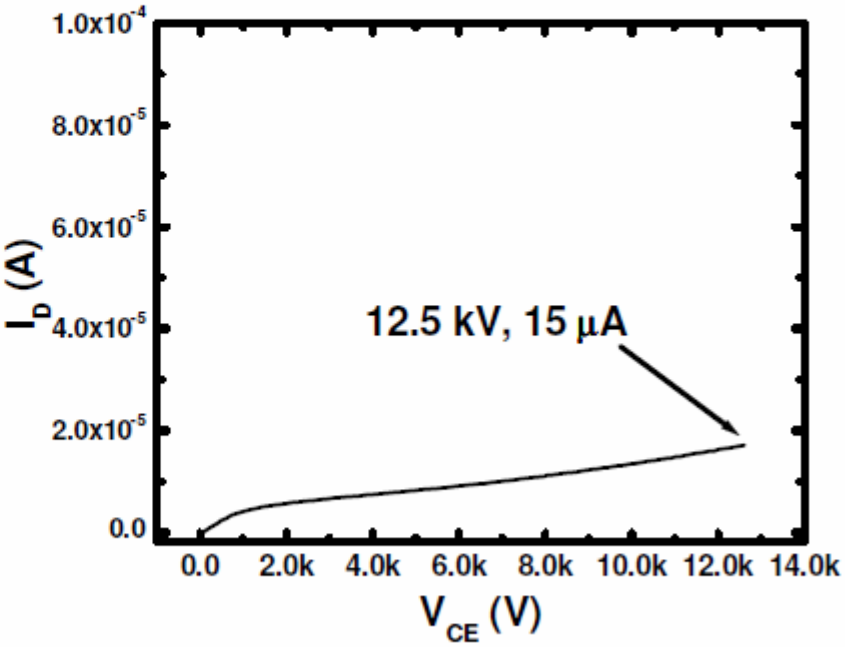
12.5 kV nチャネルIGBT (Cree)

4H-SiC *N-IGBT* Characteristics (RT)

$R_{on,sp}$ = 5.3 mΩ-cm² !!



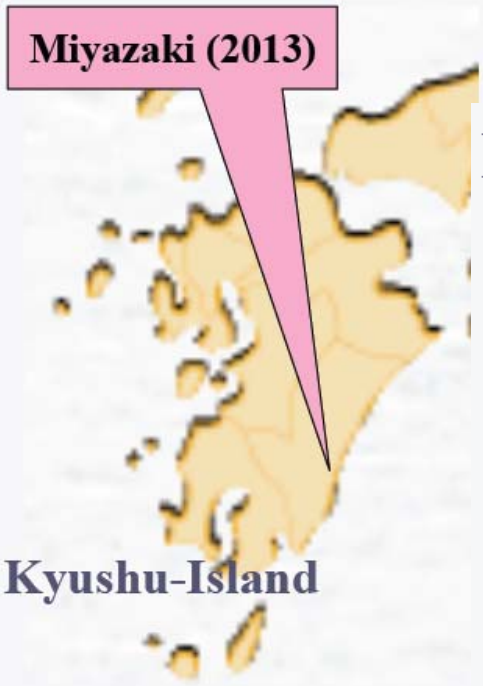
V_F = 4.1V @ 5 A, V_{GE} = 20V
= 6.1 V @ 32 A (200 A/cm²)



12.5 kV blocking (V_{GE}=0V)

$R_{on,sp}$ = 5.3 mΩ-cm²
(V_{GE}= 20V, V_{CE}= 6.1V)

ICSCRM 2013 in Japan



Miyazaki

A place of scenic beauty, Japanese ancient myth

PHOENIX SEAGAIA RESORT

Venue : Seagaia Convention Center

Date : Sept. 29 – Oct. 4, 2013